REMARKS/ARGUMENTS

Claims 1-21 are pending in this application. Claims 5, 12, and 19 have been amended to make editorial corrections to address the examiner's section 112, second paragraph rejections. Support for the amended claims is found in the specification. No new matter has been added.

Rejections Under Sections 102 and 103

Claim 1-3, 5, 7-10, 12, 14-17, 19, and 21 were rejected under section 102(b) as being anticipated by U.S. patent 5,276,899 (Neches). Claims 4, 6, 11, 13, 18, and 20 were rejected under section 103(a) as being unpatentable over Neches. Reconsideration and allowance of the claims are respectfully requested for the following reasons.

Claim 1 recites "serially receiving, from a source, a plurality of forward messages each addressed to one of a plurality of destinations." Neches does not show or suggest this feature of the invention. In Neches, requests from the host computer are communicated to an interface processor, which determines where to route the request. See Neches, column 5, lines 22-37. In contrast, in the present invention, the source transmits forward messages to the destinations (see also figure 1 of the patent application), and therefore, from the source, each forward message is addressed to one of the plurality of destinations. Therefore, the invention provides a more efficient technique of interconnecting multiple processors because an interface processor is not needed. An interface processor may introduce additional delays which the present invention does not have. For at least this reason, claim 1 of the invention should be allowable.

Claim 1 further recites "simultaneously receiving, after a predetermined period of time, a plurality of reverse messages from the destinations, each reverse message corresponding to one of the forward messages simultaneously sent to an available destination." Neches does not show or suggest this feature of the invention. Neches does not describe from each destination, simultaneously transmitting reverse messages corresponding to the forward messages. In fact, Neches describes responding processors outputting in successive packet contention time

intervals. See Neches, column 5, lines 38-62. The present invention provides an efficient interface for a steady supply of memory transactions and for "bursty" demand for memory transactions, which improves improves performance in an efficient way not taught or suggested by the prior art. For at least this additional reason, claim 1 should be allowable.

Claims 2-7 are dependent on claim 1 and should be allowable for at least similar reasons as discussed for claim 1.

Claim 8 recites similar features as discussed for claim 1 above and should be allowable. Claims 9-14 are dependent on claim 8 and should be allowable for at least similar reasons as claim 8.

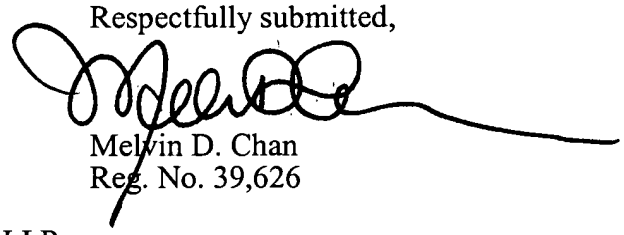
Claim 15 recites similar features as discussed for claim 1 above and should be allowable. Claims 16-21 are dependent on claim 15 and should be allowable and should be allowable for at least similar reason as claim 15.

CONCLUSION

In view of the foregoing, applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400, extension 5213.

Respectfully submitted,



Melvin D. Chan
Reg. No. 39,626

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
MDC:km
60278343 v1